A Discrete Ferroelectric Memory using a Basic Stamp Microprocessor

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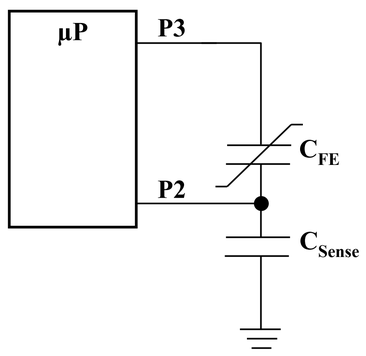
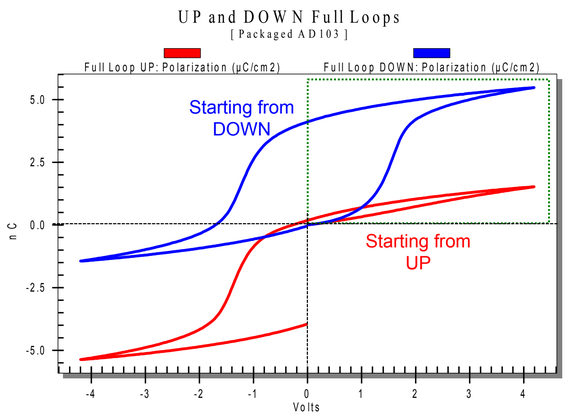
Introduction

A ferroelectric capacitor exhibits remanent polarization allowing it to be used as a non-volatile memory. The charged state of the crystal lattice of a ferroelectric capacitor is a *natural* characteristic of the material. It need only be pointed in the desired direction by the application of the appropriate voltage. A ferroelectric capacitor maintains memory without support from a battery or the environmental protection of a package. A package is needed only to facilitate handling.

Non-volatile memory based on ferroelectricity is *charge-based*. Its state is destructively read by counting electrons coming from the capacitor when it is forced into a known direction. Ferroelectric hysteresis is typically shown as a full loop, implying continuity. Memory *is intrinsically discontinuous!*

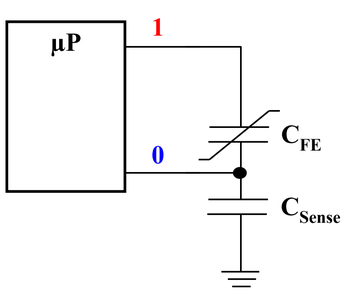
The charge coming from a ferroelectric capacitor is most easily converted to a voltage by a linear capacitor in series with the ferroelectric capacitor, hence the Sawyer-Tower circuit [1]. Taking advantage of the unique property of microprocessor pins whereby they can act either as *active outputs* or as *high impedance level-sensing inputs*, a ferroelectric memory bit may be created by connecting a Sawyer-Tower circuit to two I/O pins of a microprocessor.



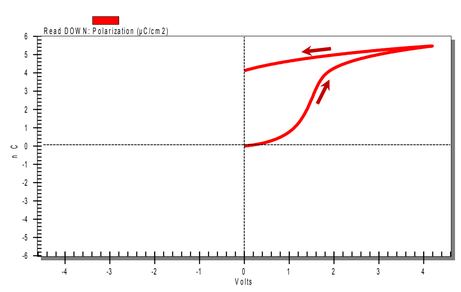


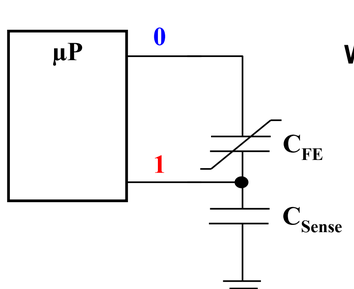
To execute these loops on a Radiant EDU, select "Standard Bipolar". To execute these loops in Vision, select "Standard Bipolar", "No Preset", and "Auto-amplification Off".

Write a datum by setting a 1:0 combination on the two I/O pins. Read the datum by setting as an input the I/O pin connected to the sense capacitor of the Sawyer Tower circuit and then applying 5V to the pin connected to the top of the circuit. Proper selection of the sense capacitor causes the sense capacitor voltage to be below the threshold for logic zero or above the threshold for logic 1.

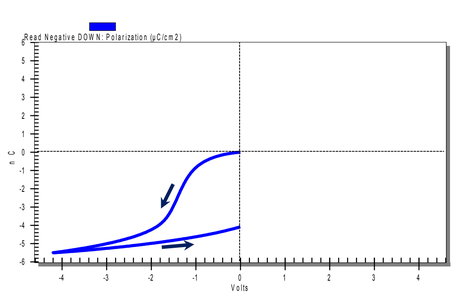


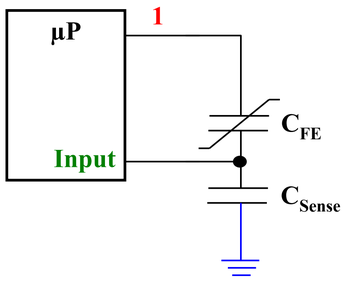
Write UP



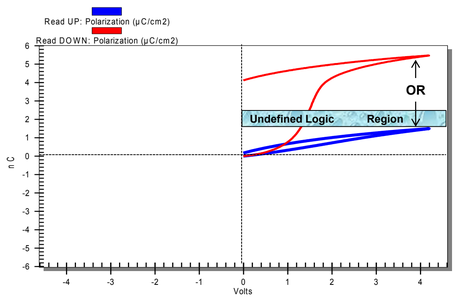


Write DOWN





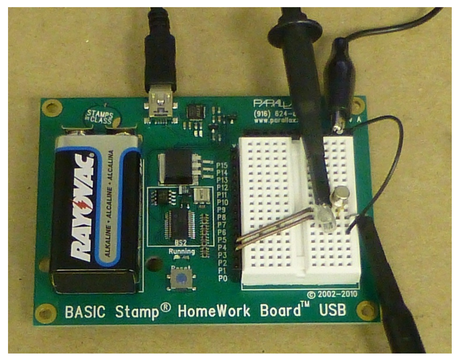
Read



To execute these half-loops on a Radiant EDU, select "Standard Monopolar". To execute these loops in Vision, select "Standard Monopolar", "No Preset", and "Auto-amplification Off".

Microprocessors

The Basic Stamp® microprocessor by Parallax (www.parallax.com) can be configured to work with the Type AD ferroelectric capacitor as a memory bit. This microprocessor is available from a variety of sources including Radio Shack. It is inexpensive, has 5 volt I/O pins, interprets the Basic programming language, and is easy to program from any PC by USB connection. The write and read operations consist of setting the I/O pins in the proper order:



Write UP

```
'Condition: :  BS2 always powers up with all pins as TTL logic inputs. Initialize pins to LOW.
   OUT3 = 0
   OUT2 = 0

 'Write "UP":  set both pins as outputs, cycle  TOP  pin high/low.
   OUTPUT 3
   OUTPUT 2
   HIGH 3
   PAUSE 1    '1ms delay to shape oscilloscope image.
   LOW 3
'Retain with pins as inputs.
   INPUT 2
   INPUT 3
'Write message to host computer screen.
   DEBUG "Write UP.", CR
   END
```

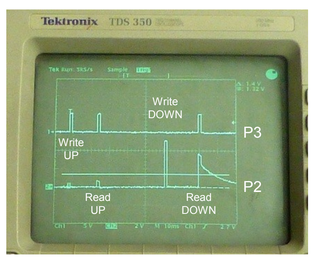
Write DOWN

```
'Condition:  BS2 always powers up with all pins as TTL logic inputs. Initialize pins to LOW.
   OUT3 = 0
   OUT2 = 0

'Write "DOWN":  set both pins as outputs, cycle BOTTOM pin high/low.
   OUTPUT 3
   OUTPUT 2
   HIGH 2
   PAUSE 1    '1ms delay to shape oscilloscope image.
   LOW 2
'Retain with pins as inputs.
   INPUT 2
   INPUT 3
'Write message to host computer screen.
   DEBUG CR, "Write DOWN.", CR
   END
```

Read

```
   fecap VAR Bit
'Start with both pins as inputs
   OUTPUT 3
   HIGH 3
   fecap = IN2
   PAUSE 1    '1ms delay to shape oscilloscope image.
   LOW 3
   INPUT 3
'Write result to host computer screen.
   DEBUG "Capacitor on READ is = ", DEC fecap, CR
   END
```

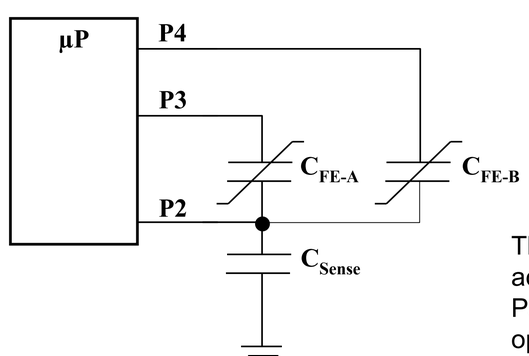


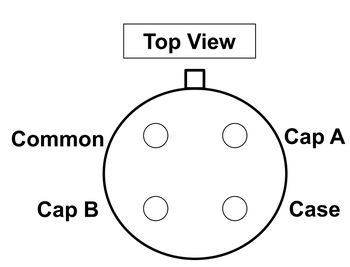
Capacitor Properties

The circuit operation shown in the oscilloscope image above was achieved using a capacitor with 10,000 square microns of area (AD103) and a 1nF sense capacitor. For detailed information on how to select the sense capacitor and mathematically determine circuit performance, go to www.ferroemems.com and click on the link for "Introduction to the FeMem". For information on long term reliability, click on the link "Ferroelectric Capacitor Properties".

Two Bits instead of One

The Type AD capacitor package contains two identical capacitors. By connecting the second capacitor to its own I/O pin, a two-bit non-volatile memory is created.





The same subroutines as above are used to access either capacitor in the package using P3 or P4 to select the capacitor address. P2 operation remains the same. If accessing P3 then P4 must be set as an input to prevent voltage application across the P4 capacitor from the P2 node. If accessing P4 then P3 must be set as an input.

Conclusion

Once the single-bit or two-bit FeMem has been constructed, you can perform a variety of experiments or use the memory in the operation of the microprocessor. You can also remove the package from the circuit after writing data and carry it in your pocket without losing the stored information.

References:

[1] C. Sawyer and C. Tower, Rochelle Salt as a Dielectric, Phys. Rev, vol 35, Feb 1930, p. 269