Introduction to the Ferroelectric Memory
Rev E
Date: April 19, 2016
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If you have a microprocessor handy, it is easy to operate single bits of non-volatile memory using a ferroelectric capacitor connected to the microprocessor input-output pins. A simple-to-implement Sawyer-Tower circuit will do. This application note explains the nature of ferroelectric capacitors, the Sawyer-Tower circuit, the operation of the Sawyer-Tower circuit using microprocessor IO pins, and how to integrate capacitor reliability considerations into circuit design decisions in case you want to retain the datum for a long time.

Ferroelectricity and FeRAMs
There exist families of special dielectric materials with non-linear properties that impart memory to capacitors fabricated with those materials sandwiched between the capacitor plates. These materials are referred to as “ferroelectric”, meaning they have permanent internal polarization that may be re-oriented by an external electric field. The capacitor will exhibit no voltage across its plates even though it is charged. The first thing I did as an electrical engineer when I tested my first ferroelectric capacitor in 1985 was to measure the voltage across its plates after forcing remanent charge in the capacitor to switch. I scratched my head trying to understand how the capacitor could show zero volts. That seemed to violate all of the principles I had learned while gaining my degree. The physics are simple: 1) charge on the plates cancels the remanent electric field inside the ferroelectric material so 2) there is no net unbalanced electric field and thus 3) no force to move charge between the plates across a short circuit. However, apply a high enough voltage to the capacitor and the remanent polarization will switch directions, forcing a rebalance of the charges on the plates and creating a dynamic event that can be recorded by external circuitry. Any event that changes the amount of remanent polarization inside the capacitor can be detected, including a change to the capacitor of net force (piezoelectricity) or temperature (pyroelectricity). Ferroelectricity is a thermodynamic state so all responses are reversible. Changing the remanent polarization inside the capacitor will cause the capacitor to generate a physical force (piezoelectric actuators) or change its temperature (electrocaloric effect), probably both at the same time.

Arne Lüker formerly of the Department of Physics at the Instituto Superior Técnico in Lisbon, Portugal has written an excellent history of the science of ferroelectricity. It is available as a PDF on the web at

http://www.arne-lueker.de/Objects/work/ferroelectrics_introduction/Ferroelectricity_History.pdf
Below I summarize Lüker’s history and include some of his references in case you wish to investigate further. Rummaging through historical technical papers in a university technical library is an amazingly satisfying experience for an engineer.

The first of these materials to be studied and measured was investigated by none other than Madame Curie’s husband Pierre and his brother Jacques as early as 1880. [Compt. Rend., 294-295, (1880)]. They studied the piezoelectric properties of the Salt of La Rochelle, a patent medicine invented 200 years earlier by Pierre and Elie Seignette [Maurice Soenen, La Pharmacie à La Rochelle. Les Seignettes et le sel polychreste, Thèse de doctorat de l’Université de Bordeaux, 1910]. All ferroelectric materials are piezoelectric as well as pyroelectric but not all piezoelectric or pyroelectric materials are ferroelectric. It was not until 1920 that Dr. Joseph Valsek at the University of Minnesota published the first electrical hysteresis loop of Rochelle salt in the Physical Review journal [Phys. Rev. 15, 537 (1920) and 17, 475-481, (1920)], solidifying the concept of ferroelectric properties. Some of the greatest names in physics like Debye, Schrodinger, and Landau contributed to the understanding of these unique but seemingly ubiquitous materials. Schrodinger is credited by Lüker with coining the term “ferroelectric”. The result is a modern materials technology embedded in memories, medical ultrasound sensors, infrared cameras, sonar, motion detectors, and diesel fuel injectors.

A recent advance in semiconductor memories arises from embedding ferroelectric capacitors into CMOS memory circuits to produce the FeRAM (Ferroelectric Random Access Memory). The internal circuitry of FeRAMs is quite complex, centered on an X/Y array of tiny ferroelectric capacitors. Because the memory effect is intrinsic to the natural state of the ferroelectric material, the memory circuitry only applies voltages to the memory array of capacitors when it needs to write or read data! At all other times no power is consumed by the memory array, highlighting one of the primary advantages of FeRAM in the IC world: extremely low energy consumption to obtain non-volatility. The rest of this document describes the basic operating principles of ferroelectric memory. Ferroelectric properties operate over all size scales from nanometers to centimeters so the principles that apply to FeRAM ICs also apply to single bits of memory stored in discrete ferroelectric capacitors.
Ferroelectric Capacitors as a Component

The equation for a classic linear capacitor is

\[
\text{Charge} = \text{Capacitance} \times \text{Voltage} \tag{1}
\]

or

\[
Q = CV \tag{2}
\]

Applying a triangle wave voltage to a linear capacitor while measuring how much charge comes out of and goes back into the capacitor results in the following graph. This is called a “hysteresis measurement”. Please note that a linear capacitor has no hysteresis but zero hysteresis is still hysteresis.

Fig 1: Q vs V plot of a linear capacitor

Equation 2 is a linear equation where the slope coefficient “C” does not change. Such a coefficient yields the straight line with slope “C” measured in Figure 1. Note that the measurement in Figure 1 is completely different than that of a capacitance meter. A capacitance meter simply gives the numerical value for C. The hysteresis measurement in Figure 1 is different in that it counts and plots every electron as it enters or leaves the capacitor during the stimulus. The hysteresis plot is far more capable of identifying non-linear properties than a capacitance meter which always assumes linearity.

Much of the charge that comes out of the capacitor in Figure 1 arises because the dielectric material between the plates of the capacitor attempts to cancel the electric field generated from the applied voltage. It does so by developing internal electric dipoles arranged in the opposite direction. These internal electric dipoles are referred to as “polarization”. As they come and go
inside the dielectric material attempting to cancel the external electric field, more charge is attracted to the capacitor plates than would be if only a vacuum existed in place of the dielectric material. A ferroelectric material differs from a dielectric material in that it has *permanent* dipoles that exist even when the applied voltage is zero. These permanent electric dipoles have two important properties:

1) Electric charge must remain on the plates of the capacitor even with zero volts across the capacitor in order to cancel the electric fields produced by these permanent dipoles and

2) The dipoles can be re-oriented by an external electric field if that field is strong enough. The dipoles remain in their new orientation after removal of the external field.

These two properties cause a dramatic change in the shape of the charge vs voltage plot when a ferroelectric capacitor is tested.

![Q vs V plot of a ferroelectric capacitor](image)

*Fig 2: Q vs V plot of a ferroelectric capacitor*

Note that the origin of the plot is in the center of the loop and that at zero volts the capacitor has two non-zero charge states. The two charge states occur where the blue hysteresis loop crosses the Y-axis. These are called *remanent* states. These remanent states will be referred to as UP and DOWN in the remainder of this document. In technical terms, these two states represent the positive and negative *remanent* charge values for the capacitor. The ferroelectric capacitor in
Figure 2 has 2.6nC of remanent charge. Switching the capacitor from one state to the other causes 5.2nC to move between the plates. The doubled amount occurs because the state on each electrode is changing from -2.6nC to +2.6nC or vice versa.

The loop in Figure 2 can be broken into two parts: 1) the switching part and 2) the non-switching part. The non-switching part is what the capacitor does every time a voltage is applied to the capacitor. The switching part is what happens when the permanent dipoles switch direction to line up anti-parallel to an applied voltage. Therefore, if half-loops are executed in the UP direction, there are two possible shapes to the response of the ferroelectric capacitor corresponding to UP and DOWN starting conditions.

**Switched vs Unswitched Half-Loops at Room Temperature**

![Graph](image)

The two possible outcomes to the positive half-loop are determined by the state of the capacitor before the test. If the capacitor was DOWN prior to the application of the half-loop, its remanent polarization will switch when the positive voltage is applied, yielding the blue loop in Figure 3. If the capacitor remanent polarization was already UP when the positive half-loop is applied, the red trace occurs. The vertical axis is in units of charge. The difference between the two traces produces a difference in the amount of charge the test circuit sees during the voltage application. That difference tells the state of the capacitor prior to the measurement and forms the basis of its use as a memory element.

Note in Figure 3 that both half-loops start at the origin. This is a different projection of the hysteresis measurement than used in Figure 2. Figure 2 is a *theoretical* projection preferred by...
physicists. Figure 3 represents the actual charge that the external circuit will see, a representation more attuned to an engineer’s perspective. The initial zero-charge state of the external circuit must align either with the ferroelectric capacitor’s UP remanent state or DOWN remanent state in Figure 2. The charge flow seen during voltage application will be the displacement along the Y-axis from the starting position at the origin to an ending position in Figure 2. For the external circuit all excursions begin at zero.

A very important point is that after the “read” operation, the capacitor is in the UP state no matter its starting state. The read operation is destructive. If the capacitor was in the DOWN state prior to the read operation, the DOWN state must be re-written into the capacitor. Another important point is that the capacitor is symmetrical in both directions in that the same two half-loops occur in the negative voltage direction. Ferroelectric capacitors with symmetrical electrodes may be physically reversed in the circuit with no change in circuit operation. However, the datum stored in the capacitor at the time the capacitor is turned around will be inverted on the next read operation! The stored data is a physical condition of the capacitor so the physical orientation of the capacitor in the circuit makes a difference. In summary, using a ferroelectric capacitor as a memory element requires the following three operations:

1) Write the UP or DOWN state using positive or negative voltage across the ferroelectric capacitor.

2) Read the state of the capacitor by applying a voltage in only one direction while monitoring how much charge comes out.

3) If the capacitor switched during the read operation, re-write the opposite state. This step is not necessary if the capacitor did not switch during the read operation.

Sawyer-Tower Circuit

The measurements of piezoelectric and ferroelectric materials by Pierre Curie and Joseph Valesek respectively were made without the benefit of modern electrical instruments. They used such devices as quadrant electrometers and ballistic galvanometers. (As a reminder, trairese down to the local technical library and look up these early instruments. Amazing!) Sawyer and Tower [Phys. Rev 35, 269 (1930)] modernized the measurement procedures for ferroelectric materials. They used the capacitance of the steering plates of a cathode ray tube to measure the charge flowing to/from the ferroelectric material. At the time, the cathode ray tube was a new lab instrument. The modern version of their circuit is shown in Figure 4.
Although the circuit in Figure 4 consists of two capacitors in series, the traditional series-capacitor equation cannot be used to determine the voltage at the sense terminal as a function of the voltage applied to the stimulus terminal. The reason is that the amount of charge the ferroelectric capacitor generates for a given voltage on the stimulus terminal is not predictable beforehand without knowledge of the capacitor’s immediate history. Think of this as an expression of Heisenberg’s Uncertainty Principle extended to macro systems. The one equation that is known is the conversion of the voltage at the sense terminal to the amount of charge that comes out of the ferroelectric capacitor. By scaling the sense capacitor value correctly relative to the size of the ferroelectric capacitor, the ferroelectric capacitor can always be operated in the saturated mode and only two charge values apply: the switching charge and the non-switching charge.

Rearranging Equation 2 yields Equation 3.

\[ V_{\text{Sense}} = \frac{Q_{\text{Ferroelectric}}}{C_{\text{Sense}}} \]  

(3)

Considering only the switched and non-switched states, the two voltages expected at the sense terminal can be defined. (See Figure 3 for the definition of \( Q_{\text{Switched}} \) and \( Q_{\text{Unswitched}} \).)

\[ V(\text{DOWN}) = \frac{Q_{\text{Switched}}}{C_{\text{Sense}}} \]  

(4)

\[ V(\text{UP}) = \frac{Q_{\text{Unswitched}}}{C_{\text{Sense}}} \]  

(5)

The steps for writing the switched and non-switched states into the capacitor are:

1) \( \text{UP} \Rightarrow \text{Stimulus Terminal} = +V \quad \text{Sense Terminal} = \text{Ground} \)

2) \( \text{DOWN} \Rightarrow \text{Stimulus Terminal} = \text{Ground} \quad \text{Sense Terminal} = +V \)
The steps for reading the switched and non-switched state are:

1) Apply +V to the Stimulus Terminal with high impedance attached to the Sense Terminal

2) Measure the sense voltage on the Sense Terminal

3) If the Sense Voltage is close to V(UP), do nothing else.

4) If the Sense Voltage is close to V(DOWN), implement a write operation to re-set the ferroelectric capacitor to the DOWN state.

During the read operation, the voltage measurement instrument attached to the sense terminal must have a high impedance input so the sense capacitor does not discharge before its voltage is measured. The minimum value of the impedance required for the sense terminal node depends upon the speed of the read operation and the value of the sense capacitor. A read operation that takes only 10 microseconds will allow a lower impedance value on the sense terminal than a read operation that requires 1 second.

NOTE: It is important to realize at this point that the ferroelectric capacitor always “remembers” its condition and does not lose its memory whether the read operation takes place in 10 microseconds, 10 seconds, or 10 years. The sense capacitor is a linear capacitor that has no memory and will lose its stored charge through any leakage path it can find. The sense capacitor and the impedance of the circuitry that reads it are the weak points in a ferroelectric memory with respect to operating frequency.

Sawyer-Tower circuits have one disadvantage. The voltage across the ferroelectric capacitor is determined by the difference between the voltage applied at the stimulus terminal and the voltage generated by the sense capacitor at the sense terminal. Complexity arises from the fact that the voltage generated by the sense capacitor is determined by the state of the ferroelectric capacitor and might have a wide range. Therefore, as a general rule when designing Sawyer-Tower circuits for memory, Equation 6 applies.

\[ V_{\text{Stimulus}} \geq V(\text{DOWN}) + V_{\text{Saturation}} \]  

\( V_{\text{Saturation}} \) is the voltage level required to fully switch the ferroelectric capacitor, approximately 2.5 volts in Figure 3. \( V(\text{Down}) \) will appear across the sense capacitor in series with \( V_{\text{Saturation}} \). Thus the stimulus voltage must be greater than the sum of the other two voltages to ensure saturated operation. The size of the sense capacitor relative to the amount of DOWN charge that comes out of the ferroelectric capacitor determines \( V(\text{Down}) \). If the sense capacitor is too small, it will generate too much voltage, coming too close to the Stimulus Voltage and preventing the ferroelectric capacitor from reaching its switching voltage. In summary, when the READ and
WRITE voltages are fixed as is the case for a microprocessor I/O pin, the saturation voltage of the ferroelectric capacitor must be less than the maximum voltage the pin can generate and the size of the sense capacitor must be carefully considered.

**Ferroelectric Capacitor Specifications**
Because a single ferroelectric capacitor can generate a wide range of charge at the same voltage, it cannot be specified by a single capacitance value as can linear capacitors. Radiant utilizes three physical properties of ferroelectric capacitors to specify the charge they will generate and at what voltage.

The first property is set by the type of materials from which the capacitor is constructed.

The materials used in the capacitor determine the shape of the hysteresis loop. Is the loop square, soft, or slim? Does it have memory or not? Is it fast as in gigahertz or slow as in milliseconds? Does it leak internally at slow speeds? At what temperature does it forget its stored data? Is it photosensitive, pyroelectric, or piezoelectric? At what voltage does it breakdown? What is its reliability? What happens at helium temperatures? All of these specifications are affected by 1) the composition of the ferroelectric material used as the capacitor dielectric layer and 2) the composition of the electrodes on either side of the ferroelectric layer. The two electrodes do not have to be the same material. Capacitors exist in research laboratories where one electrode is metallic, the other is a conductive metal oxide, and the capacitor layer consists of alternating layers of different ferroelectric compositions! Given that there are thousands of known ferroelectric materials, the envelope that defines the shape and properties of the hysteresis loop of a ferroelectric capacitor is for all practical purposes infinite.

The second property of a ferroelectric capacitor is its thickness.

The thickness of the capacitor does not affect the shape of the capacitor but it affects the voltage required to generate the saturated hysteresis loop. Ferroelectric materials respond to electric field. Electric field is defined as the voltage divided by the distance between the capacitor plates. If the thickness of a capacitor is doubled, the voltage must be doubled to maintain the same electric field strength and the same hysteresis loop shape. In summary, the thickness of the capacitor determines $V_{\text{Saturation}}$.

The third capacitor property of interest is the area of the capacitor.

The amount of charge that a particular capacitor type generates varies linearly with the area of the overlap of the top electrode to the bottom electrode. If the area of the capacitor is doubled, the capacitor will generate twice the amount of charge at the same voltage. The area of the capacitor does not affect the switching voltage of the capacitor or the hysteresis shape but it does determine the amount of charge the external circuit must supply for the capacitor to reach a specified voltage.

Radiant presently offers one combination of ferroelectric material and electrode material for its packaged capacitors to be used for FeRAM emulation.
**Type AD** 0.14μ-thick 3/20/80 niobium-doped PZT (PNZT) with platinum electrodes.

Radiant introduced a different capacitor type several years ago for use by the ferroelectrics research community to teach students.

**Type AB** 0.26μ-thick 20/80 PZT with platinum electrodes.

The 20/80 PZT is easy to make, densifies nicely, and has a very square hysteresis loop. For the same sized capacitor as in Figure 2 above, the Type AB capacitor generates 6.8nC of charge and saturates at 3.5 volts. The negative characteristic of 20/80 PZT with platinum electrodes is that it has poor reliability specifications that allow failures to occur within hours at temperature. This makes it a great target for studying reliability mechanisms but makes it unsuitable for serious study of ferroelectric memory operation.

NOTE: At least one FeRAM manufacturer uses a composition close to 20/80 PZT in its capacitors. Their capacitors are highly reliable because the electrodes are not platinum. It is the combination of electrode type with the ferroelectric material composition that determines reliability, not the ferroelectric material composition alone.

Radiant adds niobium to PZT to create the Type AD capacitor that provides acceptable long term reliability for demonstrating ferroelectric memory operation. The Type AD capacitor generates a reasonably square loop with strong remanent polarization and will not imprint or lose retained data at room temperature for over ten years. The hysteresis loops in Figures 2 and 3 are from a Type AD capacitor. The Type AD capacitor has excellent retention performance over temperature but it does wear out with cycling. This phenomenon is known as fatigue and is discussed in more detail below. The Type AD capacitor loses approximately 50% of its remanent polarization in approximately 300,000 cycles.

The Type AD capacitor is made on a die approximately 1.4 millimeters on a side, shown in Figure 5. Multiple capacitor pairs are fabricated on each die, each pair with its own area. The capacitor area specified for a particular part determines which capacitor pair is bonded to the package leads.
The measurements in Figures 2 and 3 came from the 10,000 square micron capacitor marked in Figure 5.

To allow engineers to determine how much charge will be generated by a ferroelectric capacitor in circuit, Radiant provides plots of the switching and non-switching half-loops where the vertical axis has units of polarization. The units of polarization are \textit{microcoulombs per square centimeter} of capacitor area (\(\mu\text{C/cm}^2\)). Units of polarization are area independent and can be converted to units of charge once the area of the capacitor is known. To convert a value from polarization to charge, two steps are necessary:

1) Multiply the polarization value of interest by the area of the ferroelectric capacitor to be used.

and
2) Multiply the resulting charge value by $1 \times 10^6$ to convert microcoulombs to coulombs.

The present Radiant ferroelectric capacitors are bonded into TO-18 transistor packages. The packages are marked on the side of the lid with a label to indicate the type and area of the two capacitors in the package. The areas and capacitor type are listed in Appendix A. The plots of the switching and non-switching half loops for each capacitor type are in Appendix B and Appendix C.

The “xxx” numerical designation works in the same manner used for resistors and capacitors. The first two numbers represent integer magnitude while the third number indicates how many zeros follow the magnitude. The reference units are square microns of area. For example, a square millimeter of capacitor area represents 1,000,000 square microns. ($1000 \mu \times 1000 \mu$) Its area designation is 105, a “10” followed by 5 zeros. A Type AD capacitor with 1 square millimeter of area has the packaged designation RTAD105.

The leads of the TO-18 packages have less than 0.5pF of parasitic capacitance between them so they add almost no parasitic linear capacitance to the circuit operation. One of the four leads is connected directly to the package and lid. Grounding that lead to the circuit ground extends a Faraday cage around the capacitor. Because of the shielding, quiet measurements of capacitor charge may be made of small $100 \mu^2$ capacitors, equivalent to 10pF of linear capacitance.

Fig 6: Type AB and Type AD die wiring diagram.

The one exception to the wiring diagram in Figure 6 is the 1mm² capacitor, of which only one can fit on the 1.4mm die. For the 1mm² capacitor, both the Cap A and Cap B leads connect to the single capacitor in the package.
**Sense Voltage Calculation**

The plot in Appendix B will be used to demonstrate how to calculate the voltage at the sense terminal when a voltage is applied to the stimulus terminal of the circuit in Figure 4. The half-loops for a Type AD capacitor with an area of 100,000μ² are shown in Figure 7.

![Switched vs Unswitched Half-Loops at Room Temperature](RTAD104)

Let us specify that during the read operation, a total of 4 volts is applied to the ferroelectric capacitor by the stimulus voltage. The four volts across the ferroelectric capacitor plus the sense capacitor voltage must add up to the stimulus voltage.

\[
\text{Stimulus Voltage} = \text{Ferroelectric Capacitor Voltage} + \text{Sense Capacitor Voltage} \tag{6}
\]

If 4 volts is to occur when the stimulus voltage reaches 5 volts, then the sense capacitor must have 1 volt across it. The size of the sense capacitor can be determined from that specification once the area of the ferroelectric capacitor is given. For this example, a RTAD103 will be used. It has an area of 0.0001 cm² (10,000μ²).

Charge generated by the *switched* ferroelectric capacitor at 4V:

\[
\begin{align*}
\text{Charge} & = \text{Polarization from blue trace at 4V x Area x } 1 \times 10^6 \\
\text{Charge} & = 61 \text{ μC/cm}^2 \times 1 \times 10^4 \text{ cm}^2 \times 1 \times 10^6 \text{ C/μC}
\end{align*}
\]
Charge $= 6.1 \text{ nC}$

**Sense Capacitor Value at 1V:**

$\text{Sense Capacitance} = \frac{\text{Charge}}{\text{Voltage}}$

$\text{Sense Capacitance} = \frac{6.1 \text{ nC}}{1 \text{ volt}}$

$\text{Sense Capacitance} = 6.1 \text{nF}$

The values of the components in the Sawyer-Tower circuit of Figure 4 are now defined for 5V operation:

1) Ferroelectric Capacitor $= \text{Type AD103}$
2) Sense Capacitor $= 6.1 \text{nF}$

These values will change for a different stimulus voltage. The value of the low state in the capacitor must be calculated to establish the sensing range necessary to decide the value of the state of the capacitor. This value is more of an estimation using the simple circuit model proposed here. The low state will generate *less charge* than the high state, allowing more voltage to fall across the ferroelectric capacitor increasing the amount of charge generated by the low state. Let’s assume that the sense voltage is very small so 100% of the stimulus voltage is applied across the ferroelectric capacitor in the UP state.

**Charge generated by the *unswitched* ferroelectric capacitor at 5V:**

Charge $= \text{Polarization (from red trace) at 5V} \times \text{Area} \times 1 \times 10^{-6}$

Charge $= 16 \mu\text{C/cm}^2 \times 1 \times 10^{-4} \text{ cm}^2 \times 1 \times 10^{-6} \text{ C}/\mu\text{C}$

Charge $= 1.6 \text{nC}$

**Unswitched Sense Voltage:**

Unswitched Sense Voltage $= \frac{\text{Charge}}{\text{Sense Capacitance}}$

Unswitched Sense Voltage $= \frac{1.6 \text{nC}}{6.7 \text{nF}}$

Unswitched Sense Voltage $= 239 \text{ mV}$

The sense range will be between 239mV (UP) and 1 volt (DOWN).
NOTE: The dashed lines on Figure 6 intersect the half-loops on their bottom, upward trending portions, not on their top, downward trending portions.

A Graphical Method for Determining Sense Voltages
The UP/DOWN sense voltage ratio changes if the sense capacitor value or the stimulus voltage is changed. For instance, keeping the 5V stimulus voltage but changing the sense capacitor to 4.7nF, a commonly available discrete capacitor, not only changes the sense voltages but also changes the voltage applied across the ferroelectric capacitor for the two states. One way to zero in on the resulting UP/DOWN sense voltages is by trial and error. The other way is the graphical solution shown in Figure 8 below.

Notice that the maximum polarization on the Y-axis of the plot is 70μC/cm². For a 4.7nF sense capacitor, 70μC/cm² of polarization from a 10,000μ² capacitor would generate 1.5 volts across the sense capacitor.

Charge = 70 μC/cm² x 1x10⁻⁴ cm² x 1x10⁻⁶ C/μC
Charge = 7.0 nC
Sense Voltage = 7.0 nC ÷ 4.7nF
Sense Voltage = 1.5V

If the Stimulus Voltage is 5V and the Sense Voltage at 70μC/cm² is 1.5V, then the ferroelectric capacitor would have 3.5 volts across it. This calculation does not correlate to any specific ferroelectric capacitor, only to the value of the stimulus voltage, the value of the sense capacitor, and the value of the polarizations along the Y-axis. Executing the same calculation for 40μC/cm² yields a voltage across the ferroelectric capacitor of 0.85V.

Charge = 40 μC/cm² x 1x10⁻⁴ cm² x 1x10⁻⁶ C/μC
Charge = 4.0 nC
Sense Voltage = 4.0 nC ÷ 4.7nF
Sense Voltage = 0.85V

Ferroelectric Voltage = 5V - 0.85V = 4.15V

Of course, if the capacitor generates zero charge, then the Ferroelectric Voltage will equal the Stimulus Voltage. A table can be created showing the ferroelectric voltage and the sense voltage for a range of capacitor polarization values.
### Table 1: Sense and Ferroelectric Voltages for a 5V Stimulus Voltage and 4.7nF Sense Capacitor

<table>
<thead>
<tr>
<th>Polarization (C/cm²)</th>
<th>Sense Voltage</th>
<th>Ferroelectric Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>70</td>
<td>1.5</td>
<td>3.5</td>
</tr>
<tr>
<td>60</td>
<td>1.3</td>
<td>3.7</td>
</tr>
<tr>
<td>50</td>
<td>1.1</td>
<td>3.9</td>
</tr>
<tr>
<td>40</td>
<td>0.85</td>
<td>4.15</td>
</tr>
<tr>
<td>30</td>
<td>0.64</td>
<td>4.36</td>
</tr>
<tr>
<td>20</td>
<td>0.43</td>
<td>4.57</td>
</tr>
<tr>
<td>10</td>
<td>0.21</td>
<td>4.79</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>5.0</td>
</tr>
</tbody>
</table>

These points may be plotted on the same plot as the half loops from Appendix B. They form a line, which means that we needed only to calculate the 70µC/cm² ferroelectric voltage value and draw a line from that point to the stimulus voltage on the X-axis. This line, along with the data points from Table 1 are the operating voltages of the sense circuitry using a 5V stimulus voltage with a 4.7nF sense capacitor and a 10,000µ Type AD ferroelectric capacitor. *Where this line intercepts the UP and DOWN half-hysteresis loops represent the two read points for 1) the given sense capacitor value, 2) given stimulus voltage, 3) ferroelectric capacitor area, and 4) the ferroelectric capacitor type.*

**Switched vs Unswitched Half-Loops at Room Temperature**  
[RTAD104]

*Fig 8: Type AD sense voltage calculation.*
The two intercept points are

**5V Operation with 4.7nF Sense Capacitor**

<table>
<thead>
<tr>
<th>State</th>
<th>Voltage Density</th>
<th>VSense</th>
</tr>
</thead>
<tbody>
<tr>
<td>DOWN</td>
<td>60μC/cm²</td>
<td>1.3V</td>
</tr>
<tr>
<td>UP</td>
<td>15μC/cm²</td>
<td>319mV</td>
</tr>
</tbody>
</table>

The black operating line must be re-calculated for each combination of stimulus voltage and sense capacitor value. The green operating line in Figure 8 represents the combination of 3.3V stimulus with a 4.7nF sense capacitor. Note that the green operating line intercepts the switching curve just past the saturation point, which is why the Type AD capacitors are 1400Å thick instead of 2600Å thick like the Type AB capacitors.

**3.3V Operation with 4.7nF Sense Capacitor**

<table>
<thead>
<tr>
<th>State</th>
<th>Voltage Density</th>
<th>VSense</th>
</tr>
</thead>
<tbody>
<tr>
<td>DOWN</td>
<td>52μC/cm²</td>
<td>1.1V</td>
</tr>
<tr>
<td>UP</td>
<td>11μC/cm²</td>
<td>234mV</td>
</tr>
</tbody>
</table>

To increase sensitivity during read operations, some designers use much smaller sense capacitor values than those calculated above. The smaller sense capacitor value increases the voltage differential between the UP and DOWN states during the read operation. It also does not allow the DOWN state to fully switch. This is not an issue if the differential is detectable by the read circuit. As well, the DOWN state will be re-written after the read operation so incomplete switching of the ferroelectric capacitor does not lead to errors.
The Sawyer-Tower Circuit and the Microprocessor
The Sawyer-Tower circuit of Figure 4 can be attached to two IO channels of a microprocessor to act as a single bit of memory storage.

![Diagram of Sawyer-Tower circuit connected to microprocessor]

**Fig 9: Sawyer-Tower Circuit Connected to Microprocessor**

For traditional TTL logic levels, 0.8V is the threshold for Logic 0 while 2.0V is the threshold for Logic 1 when PA.1 is set as an input. PA.1 will have tremendous input impedance when set as an input and so it will not discharge the sense capacitor. The sense capacitor of the Sawyer-Tower circuit should be selected so that the UP and DOWN states will fall into the Logic 0 and Logic 1 ranges respectively on PA.1. The 4.7nF sense capacitor examined in the previous section coupled with the Type AD103 capacitor does not yield a proper sense margin around the logic thresholds of the microprocessor input. For TTL logic levels, the sense capacitor must be reduced in size to approximately 2.2nF or smaller.

The operation of this memory bit in Figure 9 is controlled strictly by firmware but requires the IOs to have a Hi-Z input option. The three required procedures are described below.

**Write UP:**

1) Set PA.0 and PA.1 as outputs.

2) Set PA.1 low.

3) Set PA.0 high. (UP write pulse)

4) Set PA.0 low.
Write DOWN:

1) Set PA.0 and PA.1 as outputs.
2) Set PA.0 low.
3) Set PA.1 high. (DOWN write pulse)
4) Set PA.1 low.

Retention:

1) PA.0 and PA.1 should have low outputs at all times during retention
   OR
2) PA.0 and PA.1 should be set as inputs with zero values in their output buffers.
   
   NOTE: Setting the two IOs as inputs disconnects the capacitor from the MCU. The other approach is for the two IOs to be left as outputs set to zero volts when the MCU is on but the bit is not being accessed. The choice is one of reliability during temperature excursions, explained in a later section.

Read:

The read operation described next assumes that both IO pins are already set for zero volts so they do not disturb the memory capacitor state when they are enabled.

1) Set PA.0 and PA.1 as outputs.
2) Set PA.1 as input.
3) Set PA.0 high.
4) Read logic input of PA.1. (the read pulse)
5) Set PA.0 low.
6) IF value of PA.1 is high THEN call the Write DOWN subroutine to re-write the value.

It is very important to note that when PA.0 and PA.1 are switched from being inputs to outputs that the Logic Zero value has already been entered into the IO output buffer for both. The reason
is that ferroelectric capacitors switch very fast and *any stray voltage applied to the capacitor may inadvertently wipe out the stored data state!* A wrong voltage output from PA.0 or PA.1 for even one microprocessor clock cycle may be enough to cause an error.

1) Always set the IO output buffers to zero volts when not in use even if the IO is specified to be an input at that time.

2) When executing a write operation, set the ground IO pin first and then pulse the other IO pin to high and back to ground again. Both IOs end up at ground after the pulse. This prevents a disturbance after the data is written.

3) During retention, the capacitor must have only zero volts across it at all times or it must be disconnected from the MCU IO pins without a disturb.

4) When executing a read, ensure that only zero volts is applied to both nodes of the Sawyer-Tower circuit until the read pulse on PA.0 occurs.

5) The last voltage on PA.1 should always be zero volts after any operation to forcibly discharge the sense capacitor.

**Alternative Input Options**

The example above assumed that PA.1 was a traditional TTL logic input. There are other types of inputs with different threshold definitions. The experimenter must read the documentation for the microprocessor being used to determine the nature of the logic thresholds on its inputs. For instance, CMOS logic inputs determine Logic 1/0 at 50% of Vdd. Schmitt trigger inputs only transition from one logic state to another within 0.5V of Vdd and ground. Each of these different threshold conditions requires careful consideration of the ferroelectric capacitor area and the sense capacitor value.

A very flexible situation occurs if PA.1 can be set as a high-input impedance comparator. The sense threshold between UP and DOWN can then be set to any value using the other input of the comparator as the reference. If PA.1 is an ADC input for the MCU, the threshold voltage between UP and DOWN may be assigned in firmware as required.
One issue with the circuit configuration in Figure 10 is that ADCs are designed to measure driven nodes and some actually output a trickle of current, usually in the picoamp range. The sense terminal is a high impedance capacitive node so the small ADC current may charge the sense capacitor and disturb the data state of the ferroelectric capacitor. PA.1 in Figure 10 must always be an active output set to zero during retention periods to prevent the ADC from charging the sense capacitor enough to generate a disturb voltage across the ferroelectric capacitor.

Note in the calculations from Figure 8 in the previous section that an RTAD103 capacitor with a 4.7nF sense capacitor would generate only 1.3 volts on the sense capacitor for 5 volt operation or 1.1 volts for 3.3 volt operation. These DOWN state voltages during read are not high enough to ensure reading a Logic 1 on the PA.1 input during a read operation with traditional TTL logic thresholds! A smaller sense capacitor should be used in place of the 4.7nF value given in the example for TTL inputs. Perhaps a 2.2nF capacitor would be better. On the other hand, if analog voltage sensing is available on PA.1, the 4.7nF sense capacitor is an excellent choice because the lower sense voltages ensure reaching saturation of the DOWN state during the read operation.

**Event Detection**

A unique application of the Sawyer-Tower memory bit is event detection. In event detection, a known memory state is set in the ferroelectric capacitor. An external event generator is connected to the capacitor in such a way that if the event occurs, it applies power to the ferroelectric capacitor to change that initial memory state to the opposite state even if the MCU itself is not powered! A subsequent read operation can determine if the event occurred while the MCU was not powered or was executing some other function. The power for changing the state of the capacitor comes from the event, not a power supply!

A piezoelectric voltage generator attached as in Figure 11 provides a unique example. One such generator is the LDT0-28k piezoelectric switch from Measurement Specialties. If positioned against a door, the switch will generate a voltage pulse when the door is opened. If the MCU leaves the ferroelectric capacitor in Figure 11 to the DOWN state, it can periodically read the capacitor. If it finds the ferroelectric capacitor in the UP state, it knows that the piezoelectric...
switch was activated because the door was opened. The MCU can detect that that door had been opened even if the event occurred when the MCU was powered down!

Other events such as a footstep, a flashlight, the sun rising, a device being turned on or off, or a static discharge can be detected. These events should be converted to electrical power by the appropriate electromechanical device and fed to the ferroelectric capacitor using the circuit in Figure 11.

![Event Detector](image)

**Conclusion**
The Sawyer-Tower single memory bit attached to a microcontroller creates a single-bit ferroelectric memory. (FerroMem) It is exactly the opposite of the 8 gigabyte flash keys available today, only one bit. It does however provide an excellent platform for understanding the operation of FeRAMs, an important memory technology coming of age today. The single-bit memory, which is truly non-volatile, can provide an external status indicator for the MCU or may be used to detect external physical events while the MCU is unpowered.

Radiant Technologies offers the EDU, a small, inexpensive tester, for those interested in more deeply investigating the properties of ferroelectric capacitors. This instrument can measure the packaged ferroelectric capacitors from Radiant up to size AD103 and characterize the properties of ferroelectric capacitors that may be used in your Sawyer-Tower memory. Please visit Radiant at [www.ferroelectriccomponents.com](http://www.ferroelectriccomponents.com) or contact us at 505-842-8007 for assistance.

A detailed explanation of the physical properties of ferroelectric capacitors is provided in the document “Ferroelectric Capacitor Properties” available from Radiant.
Appendix A
Capacitor Areas by Type

Types AB and AD

<table>
<thead>
<tr>
<th>Color</th>
<th>Area (cm²)</th>
<th>Alphanumeric</th>
<th>Alphanumeric</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>1x10⁻²</td>
<td>RTAD105</td>
<td>RTAB105</td>
</tr>
<tr>
<td>Blue</td>
<td>1x10⁻³</td>
<td>RTAD104</td>
<td>RTAB104</td>
</tr>
<tr>
<td>Orange</td>
<td>4x10⁻⁴</td>
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<td>RTAB403</td>
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<td>White</td>
<td>1x10⁻⁴</td>
<td>RTAD103</td>
<td>RTAB103</td>
</tr>
<tr>
<td>Yellow</td>
<td>4x10⁻⁵</td>
<td>RTAD402</td>
<td>RTAB402</td>
</tr>
<tr>
<td>Black</td>
<td>1x10⁻⁵</td>
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<td>RTAB102</td>
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<tr>
<td>Red</td>
<td>4x10⁻⁶</td>
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<td>RTAB401</td>
</tr>
<tr>
<td>Green</td>
<td>1x10⁻⁶</td>
<td>RTAD101</td>
<td>RTAB101</td>
</tr>
</tbody>
</table>

NOTE: On the earliest versions of the packaged ferroelectric capacitors, Radiant denoted the area of the capacitors bonded to the pins of the package with colors. Those original color designations are denoted in the first column.

NOTE: The “RT” will not be included on package labels.
Appendix B
Polarization Curves for the Type AD Capacitor

The Type AD capacitors are 0.14 µ thick and may be operated up to 5V for 10 seconds or shorter. The Type AD is not designed for DC operation but will withstand 4.2 volts under long term DC bias at room temperature. The Type AD is intended for operation from room temperature to 85°C and will begin to leak during hysteresis loops slower than 10 seconds at 85°C.

The Type AB capacitor has a fatigue lifetime of 300,000 cycles to 50% from room temperature to 85°C and an imprint lifetime projected to be greater than 10 years at 85°C after the initial loop.

Recovery: 5 volt square wave for 100 seconds at either room temperature or 85°C.
Appendix C
Polarization Curves for the Type AB Capacitor

Switching vs Non-switching Half-Loops
[Radiant Type AB Cap]

The Type AB capacitors are 0.26µ thick and may be operated up to 9V for 10 seconds or shorter. The Type AB is not designed for DC operation but will withstand 5 volts under long term DC bias at room temperature. The Type AB is intended for operation only at room temperature and will begin to leak during hysteresis loops slower than 10 milliseconds at 85°C.

The Type AB capacitor has a fatigue lifetime of 20,000 cycles to 50% at room temperature and an imprint lifetime projected to be 10 years at 85°C after the initial loop.

Recovery: 9 volt square wave for 100 seconds.