Ferroelectric capacitors have unique qualities as memory devices compared to all other memory media. Ferroelectric materials have memory as a natural property. In fact, they are always remembering one thing or another from the day they are made. Unlike silicon devices, they care not about being handled by humans. Sixty years of commercial implementation as discrete capacitors and piezoelectric elements proves that they are robust components. They operate over an incredible temperature range from 5 K to 500 K or higher without losing their remembered state! (See Radiant’s web site for cryogenic measurement results on PZT and PNZT thin films.)

All other solid-state memory technologies such as EEPROM, FLASH, and MNOS require that the memory devices be buried deep inside an IC for their own protection. The question arises: Given their robust properties, will ferroelectrics allow us to create memory products unlike anything in the past? The answer is “Yes!” Using ferroelectric memory capacitors in discrete or integrated circuits, it is possible now to

1) Make non-volatile solid state switches connected to the Internet-Of-Things. A non-volatile solid state switch is functionally equivalent to the mechanical light switch on the wall.

2) Add a few bits of non-volatile memory to any IC without the necessity of developing a thin ferroelectric film process fully integrated with CMOS;

3) Create bipolar non-volatile memory;

4) Create circuits that operate with no traditional power source but instead perform memory operations using scavenged energies having magnitudes far below those presently required for energy harvesting systems;

5) Add non-volatility to any electromechanical device including relays, valves, alarms, transmissions, engines and doors;

6) Create mail boxes for one microprocessor or system to leave messages for another even though the other is powered off;

7) Allow a microprocessor to detect the occurrence of external events even while the microprocessor is powered off;

8) Build true radiation-hardened memory;
9) Enable RF tags to sense the environment and report their findings \textit{without a battery} in the tag;

10) Create fully static \textit{non-volatile} CMOS logic;

11) And, create fully stand-alone autonomous counters for metering applications.

Most importantly, this technology is not covered or inhibited by any existing patents besides those owned by Radiant Technologies!

This document provides the instruction necessary to design functional and error-free autonomous ferroelectric memories. It is the culmination of 10 years of work at Radiant. The purpose of the document is to allow IC designers to achieve proper functionality and reliability on his or her first try without having to follow the 10-year learning curve. This information is public domain. Please contact Radiant with any questions.
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The Perfect Non-volatile Memory

Consider memory function from the viewpoint of a ferroelectric capacitor. Memory is intrinsic to each and every ferroelectric capacitor. Once one can build a robust ferroelectric capacitor, everything boils down to the question of how to talk to it, how to ask it what it knows. Is there a simple circuit whose operation is affected by the state of a single embedded ferroelectric capacitor? Autonomous non-volatile memory circuits are possible and turn out to be surprisingly easy to build.

Autonomous memory is a non-volatile memory bit or latch that operates independently from any controlling system. In theory, the simplest non-volatile memory stores only one bit of information and has only on three lines: power, ground, and In/Out. This theoretical autonomous memory element has only two operating rules:

1) With power on, drag the I/O terminal to the high or low logic state you want and it stays there.

2) When power leaves and returns, the last state returns.

What can be done with one bit? Who would use it? The answer is that ferroelectric capacitors can impart local intelligence to any system, sub-system, or electromechanical component. Instead of gigabits of flash memory that must have a computer present to read and write the information, there will soon exist single bits of non-volatile memory embedded in every electromechanical system and any sensor that interacts with humans. These objects will sit at the tips of the nerve fibers evolving with the IOT (Internet of Things). Ferroelectric capacitors smaller than one square micron are routinely manufactured today. Such capacitors require only a picojoule of energy to set a memory state. Exposing such capacitors to the ambient environment creates incredible opportunities for harvesting information and establishing communication between humans and electronics.
How does autonomous memory function?
A simple RC circuit built with a ferroelectric capacitor generates the following switching (blue) and non-switching (red) voltage profiles when the rise time of the voltage at the top of the in-line resistor/capacitor combination is faster than the charging rate of the capacitor.

![Fig. 1: Output of a simple RC circuit where the capacitor is ferroelectric.](image)

The test circuit I used to capture the two signals above is in Figure 2.

![Fig. 2: Measurement circuit for the results in Figure 1.](image)

The three signal connections 1) DRIVE, 2) RETURN, and 3) OSC refer to connections on Radiant’s testers and correspond respectively to the 1) stimulus voltage at the top of the stack, 2) the electrometer measurement terminal at the bottom of the stack collecting all of the charge that flows through the circuit during the test, and 3) a voltage measurement terminal. The voltage follower op amp isolates the RC node so the instrument measuring the output voltage does not disturb the evolution of the system during charging. The ferroelectric capacitor in Figure 1 is a
2600Å-thick 20/80 platinum-electroded device with an area of 400 µm² (401). The resistor is 16 MΩ.

The “shelf voltage” in Figure 1 is the item of interest. When the ferroelectric capacitor enters its switching phase, it generates more charge per incremental voltage step than before switching starts or after switching ends. This increases the effective capacitance in the circuit during switching, slowing down the rise time. When all of the remanent polarization has switched, the rise time decreases again to match that of the unswitched capacitor. The non-switching situation does not experience the dramatic increase in temporary capacitance so it does not develop a shelf. The length of the shelf is determined by the value of the resistance. The shelf voltage always occurs even in FRAMs with nanosecond-scale access times but in that case the signals are so fast that the shelf is almost invisible to measurement instruments. The shelf in Figure 1 is milliseconds long because I intentionally slowed down the operation of this circuit using a large resistor in series with the ferroelectric capacitor in order to easily capture and study the responses.

Current gain can be added to the RC circuit by placing a transistor in the circuit so that the ferroelectric current controls the conduction of the transistor. The test circuit for this arrangement is shown in Figure 3.

![Measurement circuit for the RC-Transistor circuit.](image)

Note in Figure 3 that every electron that comes out of the ferroelectric transistor goes into the base of the bipolar transistor. This will force a current equal to the transistor β times those number of electrons to flow through the emitter/collector path of the transistor. The voltage response of the circuit should have the same shape without the transistor as in Figure 1 but the length of the shelf voltage should be increased by (β+1). A comparison of the response of the two circuits with and without the transistor shows that this model is indeed true. The resistor in the base-emitter circuit of the bipolar transistor is ignored to simplify this explanation.
In Figure 4, the two green dashed lines represent the switching and non-switching trajectories of the output of the RC<sub>FE</sub> circuit in Figure 1. The blue and red traces are the switching and non-switching outputs respectively of the circuit in Figure 3 where a transistor has been added to the RC<sub>FE</sub> circuit to provide gain. The switching response of the circuit with the transistor is approximately 3.2 times longer than the switching trace of the RC<sub>FE</sub> circuit alone, consistent with my proposed (β+1) model. However, the β is only ~2 for the bipolar transistor because the current flow through its emitter/collector circuit is nanoamps.

NOTE: The RC time constants in Figure 4 are in the milliseconds. This slow speed was targeted to make it easier to capture and study the shelf voltage effect. It was accomplished by using very large resistance as the conductive load. The time frame for the read operation shown in Figure 4 can be adjusted to any scale by adjusting the values of both the ferroelectric capacitor and the conductive load to achieve the desired frequency response. Note that the shelf voltage will always occur when the ferroelectric capacitor switches, even in every FRAM capacitor, albeit at speeds we cannot measure.

The equivalent MOSFET circuit to the Bipolar circuit in Figure 3 is below:
What is not shown in Figure 3 but is in Figure 5(a) is the Reset input. The Reset input allows an external stimulus to set the ferroelectric capacitor Cdata DOWN. The resistor in Figure 5(a) is necessary to allow the Reset input to rise to its full potential in order to place Cdata in the DOWN state. This same function is performed in the bipolar version of this circuit by the resistor in the base circuit of the transistor. The value of the resistor is set so that the current through T2 is enough to turn on T1 and Cdata can switch completely entirely down during the Reset pulse. Without the resistor, the diode at T2 would prevent Reset from rising to full potential unless the saturation voltage for Cdata was below Vth for T2.

Implementing the Conductive Load and the current limiting resistor in Figure 5(a) with MOSFETs in a CMOS IC process makes the circuit look like Figure 5(b). The $V_{Bias}$ on the load transistor in Figure 5(b) puts transistors T4 and T3 in the linear mode, making them act as resistors.
Fig. 5(b): All-transistor current sensitive CMOS autonomous memory

The resistance values of T3 and T4 can be set to different levels for a single $V_{\text{Bias}}$ value by varying their relative geometries. There are a myriad of other possible load circuits that can be put in place of T3 and T4. Loads that change their impedance as a result of the circuit state would allow the circuit to reduce its current draw while holding a constant state. T3 could be changed to a simple pass gate that turns off during Reset. T1 would not turn on during Reset in that case but Cdata could switch through T4 if the Analog Output is connected to ground during Reset.

The circuits in Figure 3 and Figure 5 are not memory latches but they have their own very unique uses as event detectors. I will return to that subject later in this document.
**Non-volatile Autonomous Latches**
The bipolar transistor and MOSFET circuits above only output the memory state for a short time while power is rising. After power stabilizes, Cdata will always be UP and the output will match Power. Adding a feedback circuit to detect that short memory state allows the circuits to latch the recalled state and rewrite it at the same time.

**Fig. 6(a):** Bipolar autonomous latch

**Fig. 6(b):** MOSFET autonomous latch
The two circuits in Figure 6 are similar. Each latch automatically reads the state of the ferroelectric capacitor during power up as shown in Figure 7. Voltage applied to the Power node causes current to flow through the Conductive Load and Cdata to ground through the control port of T1. (T1 of the bipolar transistor or T1_D of the MOSFET current mirror as shown in Figure 6.)

**Fig. 7(a):** Read operation of the Bipolar autonomous latch

**Fig. 7(b):** Read operation of the MOSFET autonomous latch
This paths in Figure 7 set the rise time of node B to match the RC time constant of the ferroelectric capacitor according to the remanent polarization state of the ferroelectric capacitor. The value of the Conductive Load is set such that if the non-switching red trace in Figure 4 is followed by point B, the voltage drop across the Conductive Load is not enough to turn on transistor T2 in either circuit. The voltage across Cdata eventually reaches that of Power so T2 and T1 both remain off while the Logic Output at B goes to the value of Power. If, however, the switching blue trace in Figure 4 is followed by B, then the voltage drop across the Conductive Load will increase while power rises, turning on T2. T2 then turns on T1, pulling node B down almost to ground and latching out a low state. In either case, the latch will maintain in the recalled state until Power is removed or a new state is forced either through node A or node B.
**Automatic Re-write!**
The autonomous memory circuits of Figure 6 automatically re-write the recalled state of Cdata after power up. First, definitions:

A. “UP” means that the last voltage applied to Cdata was positive on the power side of the capacitor.

B. “DOWN” means that the last voltage applied to Cdata was positive on the bottom of the capacitor, the side connected to node A.

When Power is applied to the circuit, the voltage that grows across Cdata is in the UP direction. If Cdata is UP before power up, then it will not switch during power up and Output B will end up in the high condition with T2 off. As long as power is applied, the voltage across Cdata will maintain its UP state. If Cdata is DOWN before power up, it will switch as Power increases. The extra current from Cdata will turn on T1 in either circuit and cause Output B to hesitate, forming the shelf voltage. The shelf voltage will turn on T2 which in turn will latch T1 on. This condition will latch Output B low. It will also force a positive voltage on the bottom of Cdata, re-writing the DOWN state existing before power-up. The voltage path across Cdata in the DOWN state is shown in Figure 8 as a red dashed line for the MOSFET circuit of Figure 7(b). The green dashed line in Figure 8 shows the current path that maintains T1 on during the low output logic state. Inspection of the bipolar circuit in Figure 7(a) shows that it will operate in an equivalent fashion.

![Fig. 8: The re-write architecture](image-url)
Using Sense Capacitors instead of Current Detectors
The circuits in Figures 6, 7, and 8 require a supply voltage equal to or larger than the saturation voltage of the ferroelectric capacitor plus a diode drop from the bipolar transistor or the threshold voltage of the MOSFET T1D. Adding a sense capacitor to the circuits in Figure 9 will convert the read operation from current-sensing to voltage-sensing and lower the overall voltage required to operate the circuit. It also eliminates the need for a current mirror in the MOSFET version of the circuit.

![Diagram of Bipolar Autonomous Latch with Sense Capacitor](image)

**Fig. 9(a):** Bipolar autonomous latch with sense capacitor

![Diagram of MOSFET Autonomous Latch with Sense Capacitor](image)

**Fig. 9(b):** MOSFET autonomous latch with sense capacitor
The requirement to exceed Vth on the control node of T1 is eliminated by the presence of Csense, lowering the maximum voltage required for Power. Nevertheless, Csense will add area to the circuit. How much space will be taken by the sense capacitor if it is made from the same ferroelectric material? The answer, at least for Radiant’s PZT capacitors, is around x15 of the data capacitor.

The number can be determined from the plot of the switching and non-switching half-loops of the data capacitor. Remember that if Csense is created with a ferroelectric capacitor, it will always be in the UP state no matter what Cdata does.

![Switching and non-switching half-loops at room temperature](image)

**Fig. 10:** Switching and non-switching half-loops for 1500Å of 3/20/80 PNZT with platinum electrodes.

Assuming

A. that the threshold for the bipolar and MOSFET transistors is approximately 0.7 volts,

B. that the supply voltage is 3 volts,

C. that there is one threshold drop of 0.7 volts to Power, and

D. that the 50% remanent polarization point is considered the 1:0 divider for maximum imprint endurance,

then the calculation of the sense capacitor area given the data capacitor area is as follows.

1. The low state does not fatigue. Failure of the low state will occur only when the voltage it generates on the sense capacitor reaches 0.7 volts (in this example). Therefore, the worst case low state will be $8\mu\text{C/cm}^2$ at $[3v - 0.7v] = 2.3$ volts as shown by the gray
dashed lines in Figure 10. The worst case read voltage for the switching state will be \(52\mu\text{C/cm}^2\).

2. The polarization threshold between Logic 1 and Logic 0 is

\[
\frac{(52\mu\text{C/cm}^2 - 8\mu\text{C/cm}^2)}{2} + 8\mu\text{C/cm}^2 = 30\mu\text{C/cm}^2
\]

This means that the bit will fail when the high or low opposite state imprints to \(30\mu\text{C/cm}^2\) or the high remanent state fatigues to \(30\mu\text{C/cm}^2\).

3. Using the same capacitor type as Cdata to make Csense and assuming that this capacitor is always in the non-switching state, the 0.7 volt threshold occurs at \(2\mu\text{C/cm}^2\) as shown in Figure 10 by the short green dashed line.

4. The equation relating the areas of the data and sense capacitors is (Cdata area = 1)

\[
\text{Charge from data capacitor at 2.2 volts} = \text{Charge into sense capacitor at 0.7V}
\]

\[
30\mu\text{C/cm}^2 \times 1 = 2\mu\text{C/cm}^2 \times \text{Sense Capacitor Area ratio}
\]

\[
30\mu\text{C/cm}^2 / 2\mu\text{C/cm}^2 = \text{Sense Capacitor Area}
\]

\[x15 = \text{Sense Capacitor Area ratio}\]

In summary, adding a sense capacitor to a single autonomous latch adds an area equivalent to 15 times the area of Cdata plus its electrical connections. But, it lowers the maximum value required for Power by Vth.

There is one important note about the MOSFET version of the autonomous latch with a sense capacitor in Figure 9(b). When the latch is in the UP state putting out a high value at B, the common line connecting the bottom of T2, the bottom of Cdata, the gate of T1, and the top of Csense has no discharge path so it will float, at least for as long as a DRAM capacitor remains partially charged. Most thin ferroelectric capacitors conduct around 1\(\mu\text{A/cm}^2\) at 1 volt so a ferroelectric Csense will eventually discharge this floating line to ground and generally hold it there. There may be a reliability problem in a situation with noisy or spiky power so a fourth leg may be added to the three-legged latch in Figure 9(b) to lock that floating node low when a high logic state is output from the latch. The circuit will then look like a traditional sense amplifier but it cannot operate in the same manner. The fourth leg must either be extremely weak so that it does not overwhelm the ferroelectric signal on the base or gate of T1 or it must not turn on until after the voltage across Cdata is higher than the full switching voltage for the capacitor. The delay can be voltage sensitive or can simply be timed. An example circuit for the MOSFET is shown below. Figure 11 shows a solution using a Zener diode to set a voltage threshold. T3 in Figure 11 will only turn on if the Logic Output is high after Cdata has reached a voltage above saturation. Once on, T3 will hold the gate of T1 hard low until the latch is written to the opposite state. Other circuits may be more area friendly.
Fig. 11: Four-legged latch with voltage sensitive latching of the floating node.
Data Capacitor Geometries
The geometry of the ferroelectric capacitor embedded in the autonomous memory determines the memory’s reliability and operating voltage. The $R C_{\text{FE}X}$ circuits of Figures 6, 7, 9, and 11 essentially meter charge into the ferroelectric capacitor. The autonomous latch can be made resistant to disturbs by requiring the latch to move more charge into and out of the ferroelectric capacitor than potential disturb events can generate. For instance, I have found from handling our packaged discrete PZT capacitors that static discharge can switch the state of the smallest capacitors we make with less than 100 square microns of area but it cannot change the state of our standard development capacitor which has an area of 10,000 square microns. To make an autonomous memory latch impervious to direct disturbs, the power generated by the potential disturb events must be determined. The ferroelectric capacitor should then be sized far larger than those events. Once the capacitor area is set, the geometry or values of the other components of the latch can be determined. Autonomous latches can function in circuits operating at any voltage. The capacitor thickness simply need be adjusted appropriately.

Reliability
The autonomous memory circuit can be operated in two power modes. In the DC mode, the circuit is powered up, the memory reads its data and hands it to the circuit on its output, and the memory circuit remains powered from then on. In the case of the latches that are already powered up, the latch state can be changed in the traditional manner by external systems or circuitry and the latch will 1) retain the new state and 2) write the new state in its ferroelectric capacitor. The reliability issue here is how long the ferroelectric capacitor can withstand the DC voltage applied across it as long as Power is applied. As a minimum, the capacitor should be able to withstand the DC voltage for at least 10 years over the specified temperature range. It is possible to develop ferroelectric capacitors to withstand such a bias. If the ferroelectric capacitor technology being used cannot withstand long-term DC biases, then the second mode of operation can be implemented: the pulse mode. The autonomous memory is powered up only long enough to retrieve and re-write the stored data after which time it is powered down. In this mode, the ferroelectric capacitor must only meet the same reliability specifications already achieved by FRAM capacitors.

Reliability for thin ferroelectric film capacitors is an entire subject by itself. There have been many journal papers published concerning this issue and the industries utilizing ferroelectric capacitors for FRAM integrated circuits, surface mount capacitors, piezoelectric sensors, and other applications have extensive experience developing reliability evaluation procedures and determining performance specifications. Capacitor reliability, as opposed to circuit reliability, will not be covered any further in this document.
Multiple Means of Fabrication:
There are three levels of fabrication complexity for autonomous memory. The first is the position occupied by fully integrated ferroelectric capacitors embedded in CMOS processes for FRAM. It is not clear that FRAM capacitors can withstand DC biases for long periods but that issue can be remedied by powering internal autonomous latches only long enough to store or recall states. Using pulsed operation, almost any possible autonomous memory application can be implemented using already-production-qualified capacitors on an FRAM process.

Autonomous memory circuits can still be used without an integrated CMOS process by bump-bonding or wafer bonding a substrate holding capacitors to the target IC substrate. By separating the ferroelectric capacitor process from the IC process, thermal budgets and process steps can be used that maximize the reliability of the ferroelectric capacitor, especially under DC bias, without affecting the CMOS circuitry which is fabricated on a separate substrate. If the ferroelectric capacitor can withstand a DC bias for the specified life-time of the memory, then the circuit can be left powered for the entire period with no failure. Radiant has reached that point with its PZT capacitor process but, because of its thermal budget, our process cannot be integrated with a CMOS substrate. Radiant could, however, manufacture a non-volatile solid state switch if it desired by bump bonding our capacitors onto analog solid state switch dice.
Event Detection
An incredible aspect of ferroelectric-based autonomous memory is the fact that the ferroelectric capacitor embedded in the memory can be written to a new state while the circuit is unpowered! This opens the door to an amazing world where non-volatile memories communicate to the outside world independent of a controller. Here is how this works.

Below is the CMOS autonomous latch with a sense capacitor. It is unpowered. The Power node can be floating or it can be grounded. The ferroelectric capacitor has been set to the UP state prior to the circuit being powered down. The application of a voltage on the Input node will

1. Turn on the MOSFET T1

and

2. Switch the ferroelectric capacitor DOWN, passing current through T1.

![MOSFET autonomous latch with sense capacitor showing power-off write with Power grounded.](image)

The power applied to the Input can come from any sensor. The conditions of the write power are

1. The voltage from the sensor or must be higher than the Cdata saturation voltage.

2. The sensor must be able to deliver the enough charge to switch Cdata down.

\[
\text{Energy per Event} = V_{\text{Saturation}} \times Q_{\text{switch}}
\]
Note: both of these conditions are controlled in manufacturing by way of the thickness and area of the ferroelectric capacitor.

3. The sensor must also deliver enough energy to charge $C_{\text{Sense}}$ up to the write voltage and to account for any current flow from node B through the Conductive Load to ground at the Power node.

It is possible to record events during powered-off situations with the bipolar version of the autonomous latch in Figure 9(a) but Condition #3 requires that the sensor generating the write event deliver a lot more energy than with the MOSFET circuit in Figure 12 because the bipolar transistor must have a constant base current in order to keep it on. For a bipolar latch the write operation will need to be very fast to minimize current loss through the base circuit of T1 while for MOSFET latches the time required to execute the write will have little impact on the required energy except for losses through the conductive load. This can be mitigated by floating the Power node when the circuit is off.

The ferroelectric capacitor can also be written UP while the latch is powered off by applying energy to the output node B. In the case of the MOSFET latch, the switching charge of Cdata will charge up Csense. Depending upon how the detection threshold is set to turn on T1, the event will stop writing when that threshold is reached and T1 is turned on by the voltage across Csense. Multiple pulses may be necessary in order to fully write Cdata UP with each pulse waiting until Csense discharges from the previous write from node B. The bipolar version of the latch has an advantage in this case because the base circuit of T1 will discharge Csense (if Csense is present). In either case, writing UP with power off from point B seems to not be as efficient was writing DOWN from point A.

To use the event detector, the controlling system writes the latch to the state opposite to that which can be written by the external sensor. It then removes power from the latch. At the appropriate time, the controller powers up the latch and reads the state. If the state changed, the monitored event occurred at least once while the system was unconscious. The latch will retain that new state until it is over-written by the controller.
Event detectors do not have to be latches but can operate as the much simpler bipolar memory circuit or the CMOS memory circuit of Figure 13.

Fig. 13(a): Bipolar non-latching event detector

Fig. 13(b): CMOS non-latching event detector
For the simple non-latching memory circuits, the UP or DOWN state of the memory is embedded in the shelf voltage of Figure 4. If the shelf voltage occurs during power-up, the memory state was DOWN prior to power-up. If the shelf-voltage does not occur during power-up, the memory state was UP prior to power-up. Since the shelf voltage will always occur at $V_C$ plus a gate threshold, simple logic-level detection cannot be used to read the memory state. Instead, the controller will need a comparator or an ADC to read the output of the memory circuit at a point where the shelf-voltage should occur. Or, a buffer tuned to the voltage drop across the Conductive Load can generate logic-level output voltages corresponding to the presence or not of the shelf voltage. For the simple non-latch memory circuits, the state will always be UP after a read operation so the external event must always write a DOWN when the event occurs.

The difference between using the autonomous memory circuits or using autonomous latches is simply that the latches will retain knowledge of the occurrence of the event until re-written but the non-latch memory circuit is a destructive read. The disadvantage of the destructive read operation may be acceptable if the lower parts-count-per-bit confers an advantage.

So far I have referred to sensors as the source of the event write operation. The energy from the event” could also be created by energy harvesting circuits and stored or used directly. Event detection is a form of information harvesting! It is actually energy harvesting but the energy is so small that only the ferroelectric capacitor switching can be executed with so little energy.
Analog Counting with Event Detectors

One of the most exciting aspects of these autonomous circuits is that they are analog memories. All FRAM designs in use today are digital in nature even though the ferroelectric capacitor maintains an internal analog state. The analog nature of any ferroelectric capacitor can easily be demonstrated with any Radiant ferroelectric tester. How to utilize the analog state of a ferroelectric capacitor instead of limiting it to digital operation? The autonomous memory circuits provide one path.

I have replicated Figure 4 below.

It is easy to demonstrate that the shelf voltage occurs when the remanent polarization of the ferroelectric capacitor begins to switch. The shelf ends when the remanent polarization switching is exhausted. The shelf voltage forms because the Conductive Load in Figure 3 and Figure 5a reduces the voltage at Point B as current through the load increases during ferroelectric switching. The current through the Conductive Load is controlled by the charge generated the ferroelectric capacitor as amplified by the transistor. This negative feedback meters the remanent polarization switching in the capacitor. By slowing down the rate of remanent polarization switching, the remanent polarization can now be much more easily set precisely. Previous attempts at analog storage in ferroelectric capacitors focused on using a precise voltage to set the remanent polarization. However, the imprint/ageing mechanism causes the voltages associated with each remanent polarization state to move over time. The total remanent polarization of the capacitor, as has been published, does not change with ageing. The autonomous memory circuit uses the ferroelectric saturation voltage to move the remanent polarization. As long as the saturation voltage used is greater than the largest possible ageing shift of the hysteresis loop, the remanent polarization state can be correctly read. Therefore, by metering the charge into and out of the ferroelectric capacitor using the autonomous memory circuit, it is possible to precisely set and retrieve the capacitor remanent polarization state. Below I give a few methods for accomplishing this feat but it is by no means an exhaustive list.

1. Timed Write/Read: In Figure 4 replicated above, the remanent polarization began in the full DOWN condition and it took 2.5 milliseconds to complete its switching. The remanent polarization can be set to an intermediate point by first saturating the remanent polarization DOWN then reading it UP for a fraction of the total switching time. The
ferroelectric capacitor will go to an intermediate analog state. The state is then read by completing the read operation and measuring the remaining lifetime of the shelf voltage.

2. Voltage Pulses: By applying write pulses to the Power node of the autonomous memory circuit after the remanent polarization has been forced DOWN the circuit can count in analog! The pulses must be shorter than that needed to saturate the remanent polarization UP. An example of a count read with pulses is shown below.

![Sequential Pulse Output Voltages](image)

**Fig. 14:** Sequential sub-saturation pulses reading DOWN state. Count = 10.

One procedure to use such a counter is to set the polarization of the ferroelectric capacitor DOWN through the Input pin. Voltage pulses of a fixed width from a sensor monitoring the events of interest are applied to the Power node of the circuit. When the controller wakes up, it simply applies more pulses to the Power node until the circuit saturates up. Knowing the total pulses that can be stored in the capacitor, the controller can subtract its count to arrive at the number of pulses that occurred while the controller was powered down.

A simple implementation of an autonomous analog counter is to use the event detector circuit discussed earlier in this document but apply sub-saturation-width pulses from the sensor. A
single event detector pin on a microprocessor or an RF tag could then count multiple events while powered down. An interrupt controller can count the events immediately on power up and create an interrupt vector based on the number of events. Two or more event detector pins would allow the wake-up interrupt vector to be based on complex rules derived from the different event generators being monitored.
**Circuit Dynamics**

Without external control lines, what controls the write and read operations of the autonomous latch or the event detector? Writing needs no timing control. There are only two requirements for the write operation:

1. The voltage across the ferroelectric capacitor must exceed the saturation voltage of the capacitor to ensure all remanent polarization is pointing in one direction and

2. The voltage application must deliver the necessary charge to the ferroelectric capacitor.

The act of reading the any autonomous memory circuit is governed by the RC time constant formed by the ferroelectric capacitor and the Conductive Load. For some applications, the voltage applied to the Power node of the memory circuit can have any rise time independent of the ferroelectric RC time constant without affecting function. In others, the rise time of Power must be slower than that RC time constant. For the second time I replicate below the shelf voltage plot of Figure 4.

![Fig. 4(c): The switching and non-switching output voltages of the autonomous memory circuit.](image)

A controller with an ADC input or a comparator input can read this output of the memory circuit directly by capturing the output voltage at the appropriate time. A heavy black dashed line has been added to Figure 4(c) above to indicate the voltage applied to the power node of the simple memory circuit. The power voltage has a very high ramp rate to its assigned value that significantly exceeds the ferroelectric RC rise time in the non-switching mode. For part of the time the magnitude of Power is above the output signal generated on the circuit output. This difference is of no consequence to the circuit operation if an analog detector is applied to the circuit output and takes its measurement after the shelf voltage forms. However, if the memory output drives a buffer to translate the analog voltage output values into logic levels, as shown in Figure 15, the logic output of the buffer will go high immediately upon the application of power because there is a significant voltage differential developed across the Conductive Load. The buffer output will remain high until the voltage drop across the Conductive Load drops below a threshold value. Thus, if Power climbs immediately to its assigned value, the logic high output of the buffer will remain until the voltage on node B is less than the detection threshold less than Power. The time period for this to happen will be set by the polarization state of the ferroelectric...
capacitor. By sampling the logic output of the buffer at the location identified by the gold vertical timing line in Figure 15, the state of the simple autonomous memory circuit can be detected with a digital input.

On the other hand, if the output of the buffer feeds the trigger input of a latch that cannot be changed once it is triggered, the initial high logic value occurring in Figure 15 must be avoided. This is accomplished by limiting the rise time of the power applied to the power node to a rate slower than the RC time constant of the conductive load and the ferroelectric capacitor. This timing is shown in Figure 16. It is always necessary for Power to rise in this manner for autonomous latches because the feedback link to the pull-up transistor (see Figure 8) makes this circuit a latch once memory. Any glitch on the feedback line will latch and re-write the wrong state.

Fig. 15: Logic output states for the buffer while the ferroelectric capacitor is charging.
In conclusion, the rise time of the power applied to any autonomous memory circuit whether latching or not controls the read operation and is a serious design consideration.
Sources of Error
At the beginning of this document I listed the two rules defining the function of an autonomous non-volatile memory bit.

1) With power on, drag the I/O terminal to the desired high or low logic state and it stays there.

2) When power leaves and returns, the last state returns.

There need be a third rule:

1) The state of the memory must not be disturbed for any reason.

The third rule is important because autonomous memory can be implemented as single bits of memory distributed throughout a system removed from any computer control. Individual bits might even be set manually by a human activating an event sensor such as a piezoelectric switch or a magnetically driven charge generator. No autonomous bits can ever make a mistake! Even though the autonomous memory circuit itself is very compact, a final product configuration may contain hundreds of extra transistors and other components in order to prevent upset by external transients. The stricter the reliability specification for the product, the more circuitry will be added to the defensive layers surrounding the single ferroelectric capacitor. The final product may even contain multiple autonomous bits that vote and correct the errant bits. At the extreme, lightning hitting a factory must not destroy the state of any bits controlling the position of any critical components deep inside the machinery. If this level of reliability is achieved, the architecture of control circuits within any factory or any piece of automated equipment will be altered forever. Think of the factory of the future as an FPGA. I spent about two years looking at this issue and testing circuits. I am convinced that the necessary reliability can be achieved.

The voltage applied to the Power node of autonomous circuits controls the read operation. Thus, all errors in the operation of the circuit will originate from problems with power. In some cases, the autonomous memory circuit may require external protection circuits to guard the power supplied to the autonomous memory circuit against disturbance. Below is an explanation of the four failure modes for an autonomous memory:

Minimum Power Voltage
The voltage applied to the Power node of the autonomous circuit must have a magnitude equal to or higher than the saturation voltage for the ferroelectric capacitor plus any voltage drops that occur in-line with the current path of the ferroelectric capacitor. An example of such a voltage drop is the threshold voltage for the base-emitter path of a bipolar transistor.

a. If the autonomous circuit is driven from a logic output, this is a known good voltage source with a very steep rise time. No protection will be needed for the circuit but if
a ramp is desired for the Power node then a step-to-ramp converter circuit may be employed. The following circuit is one I use in discrete circuits.

Fig. 17: Discrete circuit for generating a ramped voltage from a stepped voltage.

Bipolar transistor $T$ acts as a current source with resistor $R$ in its emitter-base circuit determining the amount of current. That current charges capacitor $C_R$ which increases its voltage according to the equation:

$$\frac{dV}{dt} = \frac{I}{C_R}$$

$$\frac{dV}{dt} = \frac{[(\text{Stepped Power} - V_{BE} - V_{Zener})/R]}{C_R}$$

The purpose of the Zener Diode $D$ is to ensure that the transistor does not turn on to start charging $C_R$ until Stepped Power has reached the saturation voltage of the ferroelectric capacitor in the autonomous memory circuit. The Zener diode is not necessary when Stepped Power comes from a logic device because it will rise to the appropriate voltage faster than the autonomous memory will charge. $R_D$ discharges the autonomous circuit in a known manner, preventing disturbances. This will be discussed in more detail later.

b. If the voltage applied to the Power node is not predictable or reliable, a situation which occurs when the autonomous memory exists stand-alone outside of an IC, there must be external protection circuitry. The reason is that any combination of voltage errors could occur that might disturb the state of the ferroelectric capacitor before it could be read. For power up and power down, four requirements exist:

1) Threshold detection to ensure that the external power source has reached a safe power-up voltage.
2) Regulation to convert the external voltage to the operating voltage of the autonomous circuit.

3) Ramp generation if the autonomous circuit requires it.

4) Discharge switches to discharge the autonomous circuit in a controlled manner once the external power supply drops below the assigned threshold voltage.

Note that for a discrete memory circuit, I found that the combination of the MAX16053 threshold detect IC with a Texas Instruments REG103 voltage regulator performed all of the functions described above. The pair performs threshold detection, regulate the output voltage, and produce a ramp of the output voltage after power-up. They also discharge the regulated voltage in a short period when the supply voltage falls below the set threshold. Using these two ICs to condition the power to an autonomous latch using a 10,000 µm² 20/80 PZT capacitor (switching time <1ns) prevented all external disturbs that I could throw at the circuit over a period of 4 months.

c. The protection and ramp functions above have been described in terms of discrete circuits. Each function, of course, can easily be implemented efficiently in an IC design.

Minimum Power Voltage Rise Time
The voltage applied to the Power node of the autonomous memory circuit (not the power condition circuit but the memory itself) cannot dwell at voltages near the capacitor switching voltage. Nor can that voltage ramp slower than the RC time constant of the switching state (DOWN). In either happens, the ferroelectric capacitor will slowly switch and prevent the formation of the shelf voltage across the Conductive Load.

a. As described earlier, for those autonomous circuits that require ramped power to operate correctly, the ramp must be slower than the RC time constant of the unswitched ferroelectric state but faster than the RC time constant of the switched state.

Latches Stable to Below \(V_C\)
For an autonomous latch already latched by a successful read, the circuit must remain latched to a power voltage below the switching voltage of the ferroelectric capacitor in order to prevent disturbs during power dips. Output power dips occur on many power supplies when they are first turned on. If the latch unlatches at or above the ferroelectric switching regime, unpredictable voltages will be applied to the ferroelectric capacitor that can result in a change of ferroelectric state. If the latch unlatches below the switching...
voltage regime, then if the power voltage dips that far and the latch unlatches, when power comes back a complete read operation will be executed.

**Power Down Quickly**

Power to the autonomous memories must be dissipated quickly on power down. Many bench-top power supplies that I tested have dips and spikes during power up but take up to one minute to fully power down when turned off. A slow power down will possibly allow the latch to go into a metastable state, applying unknown voltages to the ferroelectric capacitor.

b. The function of resistor R_D (“D” for discharge) in the ramp circuit of Figure 17 is to discharge the autonomous memory circuit quickly when power falls immediately to zero. Note, however, that the circuit in Figure 17 will not properly handle slowly decreasing input power as Zener diodes have fuzzy turn-off characteristics and might continue to enable the ramp circuit well below its Zener voltage when power is decreasing. The ramp circuit in Figure 17 works only with power supplied by a digital output.

c. The requirement in #3 above that the autonomous latch remain latched until power drops below the switching voltage of the ferroelectric capacitor is critical for eliminating the slow-voltage-drop error source.
Summary of Design Issues:

1. The rise time of Power must be slower than the charging time for Cdata through the Conductive Load for the non-switching state or the latch will go low every time.
   
   a. The need for a ramped rise on Power adds extra circuitry but only one of those circuits is needed on an IC as it can be shared by all autonomous bits on the die.

2. The latch must be designed such that in the low output state it will remain latched at a voltage below the coercive voltage of Cdata. If power only drops to a value below the coercive voltage but above selected unlatch voltage, the latch will remain latched. If power drops below the unlatch voltage, the power voltage is now low enough that when it comes back up it will execute a new read operation. This is not a factor for the high output state.
   
   a. During power down, eventually the transistors will go into the analog mode from the saturated mode, allowing voltages to be applied to nodes A and B without control.
   
   b. If the circuit unlatches above the coercive voltage of the capacitor, it is possible for a voltage to be left on node B as power drops. If the capacitor had originally been pointing DOWN towards node A, then residual voltage on node B will switch it partially back, possibly causing a read error when power is restored.
   
   c. If the latch remains latched to a supply voltage below the coercive voltage of Cdata, then the memory state of Cdata cannot be disturbed when the latch unlatches during falling power.

3. If T1 and T2 [See Figure 7(b)] do not turn on during power up because Cdata was in the UP state, the node connecting the bottom of T2, the bottom of Cdata, and the current limiting device on the input of T1 should not be allowed to float. In Figures 6 and 7, that node has a discharge path through T1D on the MOSFET circuit or the base of T1 for the bipolar circuit. If a sense capacitor is used with the MOSFET circuit of Figure 9(b), then a separate pull-down latch should be added to the line.

4. The Conductive Load can have variable impedance so it can deliver power to its output stage if Logic Output is high but limit power consumption through T1M if Logic Output is low.

5. Autonomous latches can operate either in the pulsed mode or the DC mode. In the pulsed mode, Power is only supplied long enough to let the state of Logic Output settle before the output is latched into a capture register. Power is then removed. Power consumption by the latch is greatly reduced and Cdata only need meet already-known FRAM reliability specifications. In DC operation, Power could remain applied to the latch for
the duration, meaning that $C_{data}$ must withstand 10 or more years of DC bias over the specified temperature range in order for the memory to be reliable.

a. The pulse-mode memory can be fabricated using existing FRAM processes.

b. The DC-mode memory may or may not be possible with existing FRAM capacitors. Nevertheless, DC-mode autonomous non-volatile memories can be fabricated by bumping down ferroelectric capacitors made on separate substrates where the capacitors can see a more robust processing environment without worry of affecting CMOS structures on the mother substrate.

6. The autonomous latch does not need to conform to CMOS voltages. Since the operating voltage for the ferroelectric capacitor can be changed simply by changing its thickness, the autonomous latch can function at any voltage for which the other circuit components are available.

a. For instance, many factories operate with an internal 48 volt bus to power sensors. The circuits in Figure 6 can be made to function at that voltage without need of microprocessor support. They can sit right next to the object they control and use the same power source! This saves money from not having to use a microprocessor with on-board non-volatile memory in the same location. Such a microprocessor will need conditioned power and assembly language programming.

b. Proper design of the latch (See #2) and the addition of power protection circuitry around the latch can ensure that no errors are ever induced in a stand-alone environment with dirty power.

7. Output $B$ will be sensitive to output loading during power up. If the load connected to the output draws current through the Conductive Load during power up, it may affect the read operation. Output $B$ should generally drive a high impedance input.

8. Input $A$ is connected directly to the base or gate node of $T1$. Any low impedance input to node $A$ can drive the latch to another state. Input $A$ must be isolated at all times and only connected to the outside world when a new input state is desired. The isolation is best performed by a CMOS pass gate or an analog switch.

9. Figure 6(a) makes it clear that non-volatile memory can be added to bipolar-only circuits. Non-volatility comes to Bipolar and BiMOS! Since bipolar is naturally radiation-hard, autonomous memory provides a means to achieve space-level radiation hardness.
Applications for the Autonomous Memory

Let us examine the list of possible autonomous memory applications mentioned at the beginning of this document:

1) Make non-volatile solid state switches connected to the Internet-Of-Things. A non-volatile solid state switch is functionally equivalent to the mechanical light switch on the wall.

   a. Simply put an autonomous latch on the control input of a solid state latch. The autonomous latch will be stand-alone in an unknown power environment so it will require significant power protection.

   b. NV solid state switches can be created by any IC company with an existing solid state switch even if an integrated CMOS or bipolar ferroelectric process is not available. All of the transistor, resistor, and traditional capacitor components can be added to the same die as the solid state switch and a substrate containing a single ferroelectric capacitor of the appropriate area and thickness can be bumped or bonded to the solid state switch die.

2) Add a few bits of non-volatile memory to any IC without the necessity of developing a fully thin ferroelectric film process fully integrated with CMOS:

   a. Given the overhead in addressing circuitry and timing circuitry associated with an FRAM array, there will be a breakeven point in cost and power consumption between using FRAM or autonomous latches to create small registers.

   b. Up to 800 ferroelectric capacitors can be reasonably fabricated on a separate 1mm² die and bumped or bonded to a host CMOS or Bipolar die. Companies without ferroelectric capacitor integrated into their CMOS or bipolar process can still add up to 512 bits of NV memory. Whether this approach will be cheaper than adding traditional Flash or EEPROM will depend upon each company and its product mix.

3) Create bipolar non-volatile memory!

   a. Definitely possible using bump/bond technology. Schottky diodes in the transistor contacts can be damaged by the sintering temperatures required of ferroelectric materials.

4) Create circuits that operate with no traditional power source but instead perform memory operations using scavenged energies having magnitudes far below those presently required for energy harvesting systems:
a. Autonomous memory bit, autonomous logic, and event detectors can be fabricated with ferroelectric capacitors having sub-square-micron areas so they can be activated at a pJ or less.

5) Add non-volatility to any electromechanical device including relays, valves, alarms, transmissions, engines and doors:
   
a. An extension of the NV solid state latch concept.

6) Create mail boxes for one microprocessor or system to leave messages for another even though the other is powered off:
   
a. Since autonomous latches can be designed to draw little power and occupy little space, it is conceivable to embed a dual-port 512 byte or larger memory array on a microprocessor die. One port would go to the microprocessor. The other to external pins to allow an external device to power up and write to the autonomous memory array while the microprocessor is off.

7) Allow a microprocessor to detect the occurrence of external events even while the microprocessor is powered off:
   
a. Connect an event detector or multiple event detectors to external pins on a microprocessor, FPGA, or other logic device. External events set the event detector. When the host system powers up, it reads the event detector and decides what to do based on the occurrence of the events.

   b. The event detectors could directly set the bits of an interrupt register to force the host system to issue a program vector based on external events.

8) Build true radiation-hardened memory.
   
a. Simple: make a NV bipolar memory.

9) Enhance RF tags to sense the environment and report their findings without a battery in the tag.
   
a. Low power NV registers are easily added to such devices without the need of adding Flash or EEPROM process steps to the die manufacture.

   b. Add event detectors or separately RF-powered autonomous mail boxes to the RF tag.

   c. Add an RF tag to a solid state switch to create an RF-controlled NV solid state switch.
10) Create fully static non-volatile CMOS logic.

a. Add an autonomous latch to the output of individual logic elements or every logic element in a critical logic circuit.

b. Create FPGAs or CPLDs with embedded non-volatility locally at every memory node.

![Fig. 18: Autonomous digital state monitor with global control lines Memorize and Restore.](image)

and

11) Create fully stand-alone autonomous counters for metering applications.

It is possible to implement powerful logic functions with embedded autonomous latches. One such structure is to combine an autonomous bit with a transparent latch to create an autonomous transfer function cell. The transparent latch must have a Hi-Z output.

![Fig. 19: Autonomous transfer function](image)

Switch 1 in Figure 19 allows the state to be preloaded into the transfer function. Switch 1 is then opened and Switch 2 is closed to transfer the state into the autonomous latch. S1, S2, and the transparent latch prevent race conditions for feed-forward and feed-back architectures involving the autonomous latch. For instance, by routing the output of the autonomous latch into an adder and feeding
the output of the adder back to S1, an autonomous counter can be created. Such a counter would recall a stored sum, increment it, and re-save the incremented value, *all on the energy supplied by the event being counted!* The result is an autonomous counter that counts without power and is only powered up to be read by an external controller.

![Fig. 20: Autonomous counter bit incorporating transfer function.](image)

The full adder in Figure 20 can be replaced by a different math function and the output of that function fed forward instead of back to create an autonomous data flow processor (serial data shift register with in-line math functions) that operates *only when intermittent power is available.* Thus, it is possible to create an autonomous processing circuit that could record events generated by an event sensor and perform a butterfly FFT on the set of event data so when the controller powers up it only need read already-processed results!

**More Applications**

One exciting application of event detectors is to enhance a system controller’s ability to analyze system faults. Ferroelectric capacitors write extremely fast. Autonomous memory circuits or latches associated with different subsystems of a computer system or an industrial system can be written almost instantly by fault detection circuitry in the subsystem. If the system crashes or otherwise suffers a disorderly shutdown, the controller can query the distributed event detectors deployed around the system during restart to see what fault was detected. The controller can then decide how to proceed with the restart sequence.

A similar situation occurs with security systems. Power interruptions can lead to periods when the security system controller is not aware of the secured status of the objects that it monitors. Simple event detector circuits powered by sensors attached to equipment cabinet doors can indicate if a server, for instance, was physically accessed while the security system was down.
The single autonomous memory latch has the potential to revolutionize electronics design, giving traditional IC circuitry the ability to directly respond to external events without the need of a processor to control and read sensors.

**Conclusion**
Autonomous ferroelectric memory is an open-ended technology that will create new applications and new markets in the consumer, industrial, and space environments. The autonomous memory circuit allows the ferroelectric capacitor to now be treated as a component in any electronic circuit, discrete or integrated. Electromechanical systems can now have memory and look like FPGAs. The technology enables a more efficient NV logic architecture that operates under intermittently powered conditions. It raises the distinct possibility of adding memory to any object where the memory is powered by the environment or by the human using the object. The technology can embed memory in any existing product line that heretofore has not had such a capability, product lines like analog switches or multiplexers or metering circuits. And, bipolar circuits can now have embedded non-volatile memory!

Please contact Radiant Technologies, Inc. in Albuquerque, NM at +1-505-842-8007 or radiant@ferrodevices.com with any questions.

**Applicable Patents**
1. US 8,565,000
2. US 8,760,907
3. US 8,787,063
4. US 8,824,186